2013-1339
(Reexamination Nos. 95/000,178 & 95/001,152)

United States Court of Appeals for the Federal Circuit

RAMBUS, INC.,

Appellant,

v.

MICRON TECHNOLOGY, INC.,

Appellee.

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board.

BRIEF FOR APPELLEE MICRON TECHNOLOGY, INC.

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AUGUST 28, 2013

CERTIFICATE OF INTEREST

Counsel for appellee Micron Technology, Inc. certifies the following:

1. The full name of every party or amicus represented by me is:

Micron Technology, Inc.

2. The name of the real party in interest (if the party named in the caption is not the real party in interest) represented by me is:

Micron Technology, Inc.

3. All parent corporations and any publicly held companies that own 10 percent or more of the stock of the party or amicus curiae represented by me are:

None

4. The names of all law firms and the partners or associates that appeared for the party or amicus now represented by me in the trial court or agency or are expected to appear in this court are:

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TABLE OF ABBREVIATIONS

’120 Patent	Rambus’s U.S. Patent No. 6,324,120
’898 application	Application No. 07/510,898, the original parent application to which the ’120 Patent claims priority
ACP	Action Closing Prosecution
Bennett	U.S. Patent No. 4,734,909, cited by the Board
BIU	Bus interface unit
Board	Board of Patent Appeals and Interferences (now, Patent Trial and Appeal Board)
Bowater	U.S. Patent No. 5,301,278, cited by the Board
CPU	Central processing unit
DRAM	Dynamic random access memory
iAPX	*iAPX Interconnect Architecture Reference Manual* (Intel Corp.) (1982), cited by the Board
iRAM	Intel Memory Components Handbook, published 1985, cited by the Board
JEDEC	Joint Electron Device Engineering Council (JEDEC) Standard No. 21-C, Revision 9, published 1999, cited by Micron in its reexamination request
MACD bus	Memory address, control, and data bus
MCU	Memory control unit
Micron	Micron Technology, Inc., Third Party Requester
Olson	U.S. Patent No. 4,933,910, cited by the Board
Park	U.S. Patent No. 5,590,086, cited by Micron in its reexamination request
PTO	United States Patent and Trademark Office

Rambus	Rambus, Inc., Patent Owner of the ’120 Patent
RAM	Random access memory
RAN	Right of Appeal Notice
Samsung	Samsung Electronics Co., Ltd., Third Party Requester
VBI	Versatile bus interface
VLSIC	Very large scale integrated circuit
Wicklund	U.S. Patent No. 5,159,676, cited by the Board
A__	Page in Joint Appendix
A__(xx:yy-zz)	Joint Appendix page where xx represents a column number of a patent, yy represents the initial line of cited text, and zz represents the ending line of cited text

NOTE: All emphases in this brief have been added unless otherwise noted.

STATEMENT OF RELATED CASES

Micron is unaware of any other appeals or petitions taken in this reexamination proceeding, however, there are a number of different matters pending in this Court and other courts that involve the '120 Patent.

1. The following pending cases involve the '120 Patent.

    a. *Micron Technology, Inc. v. Rambus, Inc.*, No. 1:00-cv-00792-SLR (D. Del.) (Robinson, J.). This case was remanded from Appeal No. 2009-1263, 645 F.3d 1311 (Fed. Cir. 2011). Following remand, the district court entered judgment in favor of Micron on February 25, 2013. Rambus filed a notice of appeal to this Court on March 27, 2013 which was assigned Appeal No. 13-1294.

    b. *Rambus, Inc. v. Micron Technology, Inc.*, No. 5:06-cv-00244-RMW (N.D. Cal.) (Whyte, J.).

2. The following pending cases do not involve the '120 Patent but involve patents that, like the '120 Patent, descend from the '898 application.

    a. *Rambus, Inc. v. Micron Technology, Inc.*, No. 2013-1087 (Fed. Cir.). This case is currently pending before the Federal Circuit.

    b. *Rambus, Inc. v. Micron Technology, Inc.*, No. 2013-1192 (Fed. Cir.). This case is currently pending before the Federal Circuit.

    c. *Rambus, Inc. v. Micron Technology, Inc.*, No. 2013-1224 (Fed. Cir.). This case is currently pending before the Federal Circuit.

    d. *Rambus, Inc. v. Micron Technology, Inc.*, No. 2013-1228 (Fed. Cir.). This case is currently pending before the Federal Circuit.

    e. *Rambus, Inc. v. Micron Technology, Inc.*, No. 2013-1426 (Fed. Cir.). This case is currently pending before the Federal Circuit.

    f. *Rambus, Inc. v. LSI Corp.*, No. 3:10-cv-05446-RS (N.D. Cal.) (Seeborg, J.).

g. *Rambus, Inc. v. STMicroElectronics, N.V.*, No. 3:10-cv-05449-RS (N.D. Cal.) (Seeborg, J.).

h. *In re Rambus Inc.*, No. 2011-1247, 694 F.3d 42 (Fed. Cir. 2012).

i. *Rambus, Inc. v. Rea*, No. 2012-1634 (Fed. Cir.) (oral arguments presented July 11, 2013)

I. STATEMENT OF THE ISSUES

1. Whether substantial evidence supports the Board's conclusion that claim 33 is rendered obvious over the prior art where the Board found that precharge information and operation codes containing read/write instructions were well-known and related functions, thus rendering obvious the limitation "wherein the first operation code includes precharge information."

2. If Rambus is not precluded from raising the issue,[1] whether substantial evidence supports the Board's conclusion that claim 33 is rendered obvious over the prior art where the Board found that DRAM was a well-known, if not dominant, form of a memory at the time of the claimed invention and the prior art discloses a synchronous memory device on a single chip, thus rendering obvious the preamble phrase "synchronous dynamic random access memory device" if the preamble is found to be limiting.

3. Alternatively, whether the Board erred in determining that claim 33 has priority to the '898 application, rendering JEDEC and Park unavailable as prior art, where the '898 application plainly describes the memory invention as a multiplexed bus interface, and claim 33 therefore has no written description

[1] Rambus does not appeal to this Court from the Board's decision finding claim 26 obvious. The claim language that gives rise to this second issue is found in claim 26.

support in the '898 application because that claim does not expressly require such an interface.

II. STATEMENT OF THE CASE

In this case, Micron and Samsung each submitted a request for *inter partes* reexamination of claims 26, 29, and 33 of the '120 Patent. The PTO subsequently merged the two proceedings into a single proceeding on July 21, 2009.

In the Office Action of July 22, 2009, the examiner initially rejected claims 26, 29, and 33, but subsequently withdrew the rejections over the cited prior art in an ACP issued January 29, 2010. Micron then appealed the examiner's allowance of claims 26, 29, and 33 to the Board.

In its Decision, the Board determined that the examiner erred in withdrawing the rejections of claims 26, 29, and 33 of the '120 Patent and held:

(1) Bennett rendered obvious claims 26 and 29;

(2) iAPX in view of iRAM rendered obvious claims 26 and 29;

(3) Bennett in view of either Wicklund, Bowater, or Olson rendered obvious claim 33; and

(4) iAPX in view of iRAM and Olson rendered obvious claim 33.

Rambus now appeals the Board's decision that claim 33 of the '120 Patent is obvious over the cited prior art. Since the only claim Rambus appeals to this Court is claim 33, the Board's decision on the first two listed rejections for claims 26 and

29 is final and this Court should not review the factual or legal analysis that the Board relied on for its decision on those claims.

As for claims 26 and 29, the Board concluded that the prior art rendered obvious a synchronous DRAM device that receives a read operation code which is sampled synchronously with an external clock. (A54-A61.) As for claim 33, the Board concluded that the prior art rendered obvious using a single operation code that includes both precharge information and a read instruction (A58-59 and A62-63.) In reaching this conclusion, the Board relied on the evidence of record which demonstrated that claims 26, 29, and 33 were obvious. Rambus also filed a Request for Rehearing, which the Board considered and denied.

III. STATEMENT OF THE FACTS

A. Introduction

Rambus alleges it is "uncontested that, in the twenty years before 1990, no one had conceived of a synchronous DRAM" that incorporates features recited in claim 33. (Rambus's Br. 3-4.)

In fact, iRAM, which is cited as prior art, discusses synchronous DRAM. (A2134 and 2139.) In addition, evidence of record establishes that synchronous DRAMs were known at least as early as 1972. (*See* A10046-47 (The Intel 4002 is a "RAM" controlled by two external clock signals φ1 and φ2 (*i.e.*, synchronous) and included "[i]nternal refresh circuitry [that] maintains data levels in the cells" (*i.e.*,

dynamic).)[2] Furthermore, in related litigation, the Defendants' expert provided a declaration (that was submitted as part of the record in this reexamination proceeding) that "Early DRAM interfaces could be asynchronous or *synchronous,* unclocked or *clocked*." (A10251-52 at ¶22.)[3]

B. Claim 33

Claim 33, with pertinent limitations emphasized, recite:

> 26. A *synchronous dynamic random access memory device* having at least one memory section including a plurality of memory cells, the memory device comprising:
>
> *clock receiver circuitry to receive an external clock signal*;
>
> input receiver circuitry, including a first plurality of input receivers to sample block size information synchronously with respect to the external clock signal, wherein the block size information defines an amount of data to be output by the memory device in response to a *first operation code*; and
>
> a plurality of output drivers to output the amount of data in response to the first operation code.
>
> 29. The memory device of claim 26 wherein the input receiver circuitry samples the first operation code *synchronously* with respect to the external clock signal.
>
> 33. The memory device of claim 29 wherein *the first operation code includes precharge information*.

(A110(26:30-65).)

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[2] In a related appeal, Rambus argues that Micron never relied on Intel MCS-4 Micro Computer Set as part of any proposed rejection. However, that is irrelevant as Micron relies on this evidence of record to rebut Rambus statement that synchronous DRAM was not known in the prior art.

[3] All emphasis added by appellee unless otherwise noted.

C. The Prior Art

1. Bennett

Bennett describes a highly versatile interconnection scheme to provide high performance, economical resources, and flexible configuration that was designed to become the standard interface for a "myriad [of] devices." (A1595(12:14-25).) This is consistent with the statement of Rambus's expert, Mr. Murphy. (A2475[¶54]("Bennett is directed to a flexible interface that can be used for interconnection of many different types of devices.").)

Of relevance to this appeal, Bennett describes the interconnection of "VLSI User Device[s]" over a Versatile Bus. (A1595(12:28-32); A1607(35:59-61).) Bennett states "[a] 'User' is the logics (e.g., a central processor *or a memory* or whatever.") (A1609(40:52-55); A1607(35:59-62).) Thus, despite Rambus's attempts to assert otherwise, Bennett clearly discloses that a User is a VLSIC that can be memory. (A1634 (90:43-44) ("Many, if not most, applications of VLSIC technology are likely to include memory devices.").)

Memory User devices are "passive" and "unsophisticated," unlike "sophisticated" processor User devices. (A1618(58:60-67); A1607(35:59-62); A1647(116:1-6).) In fact, Bennett's synchronous Versatile Bus does not have to be used for a sophisticated computer system, but can be used for "trivial" configurations "to pass but a single bit of data from a single master device [CPU

User] to a single slave device [memory User]." (A1597(15:42-53); *see also* A1618(57:54-59) ("a chip part – say a microprocessor – will likely be as good in one Versatile Bus network – say one containing only a single slave memory – as the next Versatile Bus network.").)

"Each Versatile Bus Interface Logics services a User as well as communicating across the Versatile Bus with other Versatile Bus Interface Logics. Therefore, an interface is presented to the User, which may be on a separate chip or, *as is more common, will be on the same physical substrate upon which the Versatile Bus logics are implemented in VLSIC*." (A1614(50:7-17); A1607(36:19-25).)

Thus, Bennett unambiguously discloses that the User can be memory and that the User and interface are both components of a single chip, as illustrated in Figure 1:

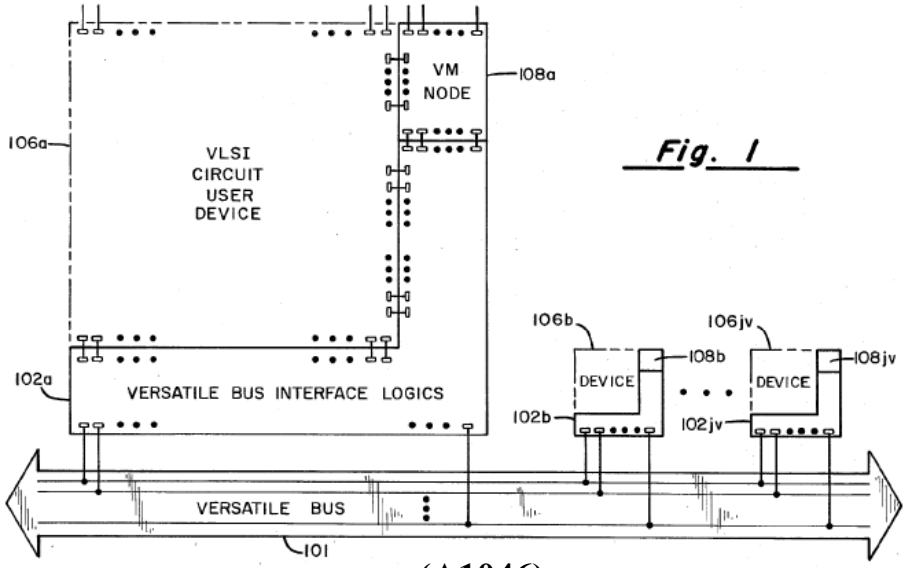


Fig. 1

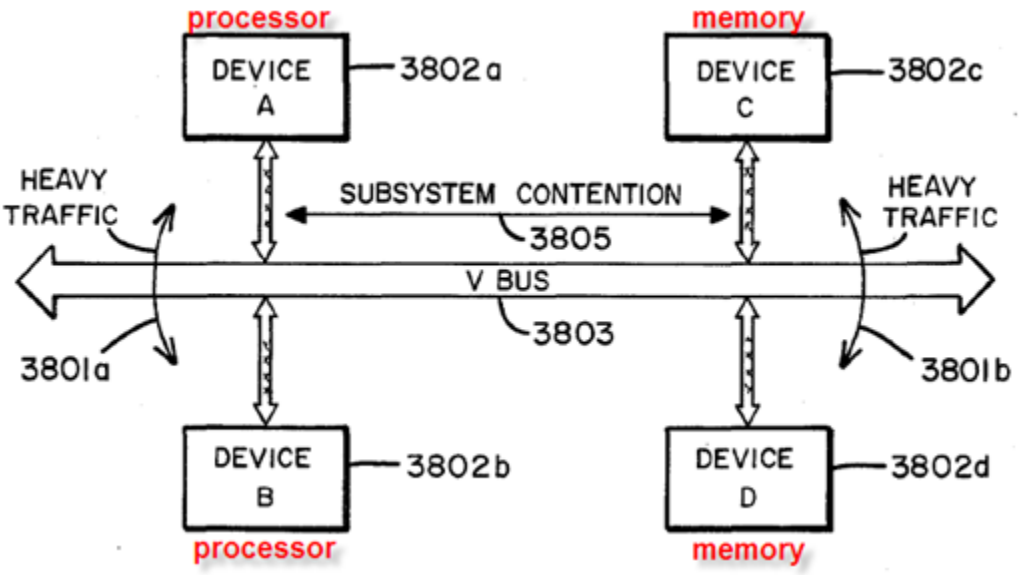
(A1046)

Rambus admits Bennett employs a synchronous Bus to interconnect the Users. (A1622-23(66:9-67:19); Rambus's Br. at 32 ("[Bennett] discloses many possible 'Users' that can be connected to the synchronous Versatile Bus.").) As noted above, Bennett clearly states that a User can be a VLSI memory device. (A1609(40:52-55); A1607(35:59-62).) These facts alone should end the issue of whether Bennett discloses a synchronous memory device.

However, to support its new argument that the claim is directed to a synchronous bus wholly internal to a chip, Rambus and its expert inexplicably assert that signals between the Versatile Bus Interface and the User would be asynchronous, even though Bennett expressly states otherwise. (A1640(101:50-54) ("The timing diagram of Fig. 52a firstly shows as reference the signals (H) ϕ1 and (H) ϕ2 *to which all communication between the Versatile Bus Interface Logics and the User*, and upon the Versatile Bus, is synchronously referenced.").) Thus, to the extent it is relevant to claim 33, the bussed communication between the memory User and the Versatile Bus Interface is synchronous with respect to an external clock signal.

As an example of how a CPU User device can access a memory User device, Bennett discloses Figure 38 where "device A and device B are processors that

predominantly respectively reference memories device C and device D" over the synchronous Versatile Bus. (A1638(97:7-10) (internal numbering omitted))



Bennett Figure 38 (A1360)(annotated)

Next, Bennett discloses two types of memories that can be used, 1) a large slow memory and 2) a small fast memory, which are well-known descriptions used in the prior art of DRAM and SRAM respectively. (A1635(92:9-14); A1733(2:18-23); *see also* A2134(iRAM)[4] and A1733(Wicklund)[5]). As discussed in the

[4] "Two basic RAM types have evolved since 1970. Dynamic RAMs are noted for high capacity, moderate speeds and low power consumption… [static RAMs] are faster and require no refresh…but the static cell's complexity puts these non-volatile chips far behind dynamics in bit capacity."

[5] "SRAM (Static Random Access Memory), which has access times as quick as one-tenth that of the DRAM's. However, that faster access time comes at the expense of a more complex device which means that it cost more, and is less dense than the DRAM."

arguments below, Bennett's teachings would at a minimum render obvious the usage of DRAM as the disclosed large slow memory.

In Figure 36, Bennett provides a detailed example of a large memory operation. (A1637-38(95:58-96:42).) The memory request is sent from a "User requester" and received by a "User large memory." (A1637(96:25-42).) In addition, Bennett provides example operation codes depicting other more complex memory operations including masked write, block read, and read-modify-write. (A1357.) For example, if an operation code indicated function number 2, the memory would be instructed to perform a read-modify-write. (A1357.) Thus, this single operation code would instruct a memory device to first perform a read, then modify the data, then automatically perform a write with the modified data. (A1635(91:13-23).)

2. iAPX

This Court previously considered iAPX with respect to similar claims in a related patent and determined that iAPX anticipated a "synchronous memory device." *In re Rambus Inc.*, 694 F.3d 42, 50-51 (Fed. Cir. 2012). The findings made in that decision regarding iAPX apply equally here.

The only different issues Rambus raises in this proceeding is the argument that "synchronous *dynamic random access* memory device" requires a single chip and the inclusion of precharge information in the operation code. While iAPX does not expressly disclose a single chip memory device or the precharge information in its operation codes, those features would have been obvious when iAPX is viewed in light of the other references relied on for the rejections.

3. iRAM

iRAM discloses an integrated RAM ("iRAM"), which "integrates all the components of a dynamic RAM memory system into a single device." (A2156.) Rambus contends that iRAM is limited to integrating only refresh circuitry. Rambus's Br. at 22 ("iRAM thus discloses combining one DRAM chip with its refresh circuitry."). However, iRAM makes it clear that its purpose is to "integrate the memory controller circuits into the memory." (A2156.) In fact, iRAM provides examples of integrated non-refresh control circuitry including "address multiplexing, and memory cycle arbitration." *Id*. There is no limitation in iRAM restricting the integration to only the refresh circuitry of the memory controller.

iRAM also provides a lengthy discussion of synchronous and asynchronous memories noting that "Intel defines a synchronous memory as one that responds in a predictable and sequential fashion, *always providing data within the same time*

frame from the clock input" and that "the 2187 iRAMs are considered synchronous devices." (A2139.) Thus, iRAM makes clear that iRAMs can be used with a memory that "provid[es] data" synchronously with respect to the external clock and does not merely refresh synchronously with respect to a clock.

While Rambus alleges this is not possible because the 2187 chip has no direct clock input, Rambus discounts the fact that the inputs to the 2187 chip are synchronized to the clock and thus can output data with respect to the clock. (A2171 (Figure 27)). Nonetheless, the specifics of the 2187 iRAM are not relevant to the rejection at issue because the rejection does not rely on the 2187 iRAM as the claimed memory device. Instead, the memory device relied on for the rejection is the synchronous MCU interface of iAPX (which indisputably has a clock input) integrated with the memory array of iAPX.

iRAM is relied on for its teachings directed to integrating a memory controller with the memory array. The fact that iRAM also teaches that it can be used for memories that are synchronous with an external clock further corroborates that one of ordinary skill in the art would apply the teachings of iRAM to the synchronous memory device taught by iAPX.

4. Wicklund

Wicklund describes memory accesses of DRAMs, specifically an improved system for well known "page mode" or "normal [or non-page] mode" accesses. (A1733-34(2:45-3:6).) In page mode, "the DRAM holds the data in the column sense amps or latches from the previous read or write operation. If a subsequent request to access data is directed to the same row [*i.e.*, page], the DRAM does not need to wait for the data to be sensed…" (A102(10:31-38); *see also* A1733(1:57-60; 2:28-39).) Simply stated, page mode results in the data maintained in the sense amplifiers and not being precharged after a memory operation.

In "normal mode" (or "non-page mode"), the data is not left in the sense amplifiers for subsequent requests and the sense amplifiers are precharged after each request. (A1733-44(2:62-3:6); A102(10:25-31).) Instead of leaving the row (page) of data in the sense amplifiers for a subsequent access as is done in page mode, a normal mode operation is followed by an automatic precharge operation. (A102 (10:47-50).)

The normal mode and page mode disclosed in Wicklund operate the exact same way as the "typical settings" for precharge described in the '120 Patent. (A102(10:50-55) ("Typical settings are 'precharge after normal access' and 'save after page mode access.'").)

Wicklund discloses that page mode is faster than normal mode if successive memory accesses are on the same row, otherwise a page "miss" time access penalty occurs. (A1733(2:45-55).) In other words, "if the new request is in a different row, that [page mode] access will actually be slower than for a standard DRAM access." (A1733(2:45-55).) This description is nearly identical to how page and normal modes are described in the '120 Patent. (A102(10:25-46).)

To address this time access penalty, Wicklund describes that "an optimal controller for page mode operation of main DRAM memory could include some means of automatically switching between page mode and non-page mode of DRAM operation depending on some prediction of whether the next access will be on the same page or on another page." (A1733(2:55-61).) When the system described in Wicklund decides to switch to normal/non-page mode, a normal/non-page mode would result in accessing data from the array followed by automatically precharging the sense amplifiers after the memory operation.

5. Bowater

Bowater describes the use of page mode to provide rapid access to data stored in a previously accessed row of memory. (A1751(6:15-17).) During a page mode access, the sense amplifiers retain previously accessed data rather than storing the data back into the array and precharging. Bowater also explains there is a maximum time that the row of data can remain open. (A1752(7:54-56; 7:62-65);

A1747.) To ensure that this maximum time is not exceeded, Bowater explains that the system sends a signal that sets a "preset value" that the counter uses to determine when to automatically trigger the sense amplifiers to store the data back into the array and precharge. (A1752(7:62-65).)

Bowater's teaching to automatically precharge when the sense amplifiers have not been refreshed in a certain time period is the same as the time period embodiment for precharge described in the '120 Patent. (A102(10:50-55) ("The DRAM can also be set to precharge the sense amps if they are not accessed for a selected period of time.").)

6. Olson

Olson also provides well-known teaching of supplying precharge information to a memory device. Specifically, Olson discloses accessing memory in either page mode (which does not precharge) or normal/non-page mode (which does precharge). A memory controller selectively activates control signals MEMPAGE and MEMCYCLE to control precharging of the memory. (A1763(2:40-44); A1764(3:28-30; 3:52-60).)

As shown in steps 54 and 56 of Olson's Figure 2, the receiving memory device (comprised of the memory array 12 and local memory controller 34) is instructed to either perform a precharge or not to perform a precharge prior to performing a read or write. (A1761; A1764(3:1-13) (no precharge on page hit as

indicated by only MEMCYCLE being inactive); A1764(3:28-41) (precharge on page miss as indicated by both MEMCYCLE and MEMPAGE being inactive).) The page memory controller determines whether or not to precharge the memory based upon a comparison of the current address with previous cycle address. (A1764(3:1-13).)

7. JEDEC

JEDEC provides a standard for SDRAM devices. (A10060; A10086; A10114.) Rambus accuses JEDEC compliant devices of infringing claims of the Farmwald patent family, which includes the '120 patent. *Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1086 (Fed. Cir. 2003) ("*Infineon*").

Although JEDEC was published in 1999 after the alleged priority date of the '120 Patent, Micron argued throughout the reexamination proceeding that JEDEC constitutes prior art because claim 33 is not entitled to a filing date earlier than February 8, 2001. (A2351-2366.)

8. Park

Park describes a "synchronous dynamic random access memory which is capable of accessing data in a memory cell array disposed therein in synchronism with a system clock from an external system such as a central processing unit (CPU)." (A10407(1:9-14).) Figures 5a and 5b of Park disclose activate, read, write,

precharge, and refresh operations and show a command that is sampled synchronously with respect to external clock CLK. (A10346.)

Although Park was filed after the alleged priority date of the '120 Patent, Micron argued throughout the reexamination proceeding that Park constitutes prior art because claim 33 is not entitled to a filing date earlier than February 8, 2001. (A2351-2366.)

D. Background of the Technology at Issue

While it appears that Rambus is attempting to provide background of the technology, Rambus actually interjects argument regarding the alleged non-obviousness of claim 33 of the '120 Patent. Given length constraints of this brief, Micron will primarily address Rambus's arguments in the Argument section (section V) of this brief.

1. Dynamic Random Access Memory

Rambus alleges that the '120 Patent improves upon prior art memory due to two features: "(1) employing a synchronous memory interface between the memory controller and the DRAMs…; and (2) using multi-bit operation codes that provide for new combination instructions that allow a controller to specify, e.g., both a read operation and whether or not the DRAM should automatically precharge as a part of the read operation." (Rambus's Br. at 7.)

Yet, none of these features is recited in claim 33. Rather, the preamble of claim 26 recites "a synchronous dynamic random access memory device" and claim 29 requires only sampling "the first operation code synchronously with respect to the external clock signal." (A110.) There is no limitation restricting the location of a synchronous memory interface. In addition, claim 33 only recites "the first operation code includes precharge information" without providing any limitation reciting a multi-bit operation code or a limitation reciting how the precharge information is used, such as automatically precharging.

Furthermore, claims 26, 29, and 33 do not recite the phrase "synchronous DRAM" that Rambus uses throughout its brief. Rather, even under Rambus's shorthand, the term should be read as "synchronous DRAM device" and not "synchronous DRAM."

Rambus does not dispute DRAMs were well-known at the time of the alleged priority date for the '120 Patent, but contends that the conventional DRAM device was asynchronous. (Rambus's Br. at 3.) Rambus urges that to determine whether a DRAM device is synchronous, "one must look to the specific bus to which *that chip* is attached." (Rambus's Br. at 10 (emphasis in original).)[6]

[6] While couched in terms of what signal a single chip DRAM device receives, this external vs. internal bus argument that Rambus relies on (Rambus's Br. at 9) was never presented to the Board in Rambus's briefs. This Court should not address arguments that were never presented to the Board. *See In re Watts*, 354 F.3d 1362, 1367-68 (Fed. Cir. 2004). Before the Board, Rambus argued only that Bennett's User device was not a single chip and the iAPX's MCU and memory array could not be integrated as a single chip, and the Board found otherwise.

However, rather than follow its own proposed construction of looking to a bus attached to a chip containing a DRAM, Rambus's arguments are premised on whether or not a bus wholly internal to a chip is synchronous.

Further, the evidence of record directly contradicts Rambus's allegations because synchronous DRAMs were known in the prior art. As discussed above, iRAM describes synchronous DRAM (A2134 and 2139) and synchronous DRAMs were known at least as early as 1972. (*See* A10047.) Finally, the expert declaration submitted in related litigation stated that "Early DRAM interfaces could be asynchronous or *synchronous,* unclocked or *clocked*." (A10252 ¶22.)

2. Precharging of Sense Amplifiers

Rambus urges that the inventors of the '120 Patent were able to achieve a more efficient memory system in part by "using multi-bit operation codes that provide for new combination instructions that allow a controller to specify, e.g., both a read operation and whether or not the DRAM should automatically precharge as part of the read operation."[7] (Rambus's Br. at 7.)

Precharging is used to help prepare a memory for a subsequent memory operation. For purposes of this appeal, the most relevant aspect of precharge is how

[7] Claims 26, 29, or 33 do not require the operation code to be "multi-bit" or that the "the DRAM should automatically precharge." Nonetheless, the prior art would still teach both of those features.

it is used in two well-known prior art modes of memory operation: 1) normal/non-page mode and 2) page mode.

First, in normal/non-page mode, the memory should be automatically precharged after a read or write is performed in order to prepare the memory for the next operation. For example, the '120 Patent acknowledges that known conventional DRAMs used precharge information before the earliest filing date of the '120 patent. (A102(10:18-21) "In normal mode (*in conventional DRAMs* and in this invention), the DRAM column sense amps or latches have been precharged to a value intermediate between logical 0 and 1.") Precharging for normal/non-page mode operation is similarly described in the prior art. (*See e.g.*, A1733-34(2:62-3:6).) In addition, Rambus stated in the underlying litigation that "the 'Read' and 'Read with Autoprecharge' described by Mr. Murphy perform the equivalent function of identifying a 'normal' mode read and a 'page' mode read." (A10031-32; *see also* A10043-44.)

Second, as described in the prior art, when a memory has been in page mode for an extended period of time, it is necessary to precharge the memory after a certain amount of time in order to avoid data corruption. (A1752(7:62-65).) The '120 Patent also acknowledges this: "The DRAM can also be set to precharge the sense amps if they are not accessed for a selected period of time." (A102(10:46-48).)

E. Alleged Objective Evidence of Non-Obviousness

Rambus purports to present "objective" secondary considerations of non-obviousness. (Rambus's Br. at 18-19.) However, Rambus's presentation of general evidence about Rambus's proprietary RDRAM product fails to establish a nexus or show that its commercial embodiment is commensurate in scope with claim 33.[8] A successful commercial embodiment does not provide objective evidence of non-obviousness unless the embodiment is coextensive with the claimed features. *Muniauction, Inc. v. Thomson Corp*., 532 F.3d 1318, 1328 (Fed. Cir. 2008).

Rambus fails to show how the alleged improvements in speed (up to 500 Mb/sec) and efficiency, or how the alleged commercial success, was due solely or even substantially to the limitations recited in claim 33, rather than other factors. Indeed, the evidence shows the exact opposite. For example, Rambus relies on its own statements that it created "'revolutionary memory chip technology … offer[ing] tenfold speed boost to memory chips,'" but never once attributes the revolutionary technology to using a synchronous DRAM device with an operation code that includes a read/write instruction and precharge information. (Rambus's Br. at 18.)

[8] Tellingly, Rambus relied upon the same purported evidence of secondary considerations in each one of 10 *inter partes* reexaminations that were pending for the Farmwald family patents. The fact that Rambus relies on the identical evidence regardless of the differing subject matter encompassed by the claims at issue in each reexamination highlights the lack of any possible nexus to claim 33.

At a minimum, those alleged breakthroughs could have been due to any number of the technologies mentioned in the specification of the ’120 Patent and/or Rambus’s RDRAM technology of the time rather than due to the features recited in claim 33. For example, the ’120 patent discloses technology for “a new bus interface” and “a clocking scheme to permit high speed clock signals” (A99 (3:22-30).) Likewise, Dr. Horowitz’s IEEE award was directed to multiple contributions to the industry and not specifically to the limitations of claim 33.

While Mr. Murphy states there was skepticism, he, as well as the materials provided by Rambus, fail to identify who exactly was skeptical. Rambus asserts that skepticism existed as to the “500 megabit per second DRAM data rate” but that rate is not recited in claim 33 of the ’120 Patent. (Rambus’s Br. at 19 (citing A2787(¶105)).) Nor has Rambus demonstrated that the features embodied in claim 33 substantially contributed to achieving that speed.

In fact, the ’120 patent primarily attributes that speed increase to the physical and electrical characteristics of the newly described multiplexed bus rather than the communication protocol used. (A99 (4:35-50 (“This high clock rate is made possible by the constrained environment of the bus. The bus lines are controlled-impedance, doubly-terminated lines. For a data rate of 500 MHz, the maximum bus 40 propagation time is less than 1 ns.”); *see also* A106 (17:61-18-

16).) Thus, even if skepticism as to 500 megabyte per second existed, it is irrelevant to claim 33.

This is particularly relevant in this instance because claim 33 merely adds using precharge information, which was already well-known prior to the earliest priority date of the '120 patent.[9] (A2337-40 (discussing precharge information in the prior art).) Even Rambus acknowledges that precharge was a well-known feature prior to the filing of the '120 patent. (A2237 (citing A2286-67).) However, secondary considerations must be based on something other than what is already known in the art. *In re Kao*, 639 F.3d 1057, 1068 (Fed. Circ. 2011) (citing *Tokai Corp. v. Easton Enters., Inc*., 632 F.3d 1358, 1369 (Fed.Cir.2011) ("If commercial success is due to an element in the prior art, no nexus exists.").

Further, Rambus relies on the testimony of Dr. Horowitz and Dr. Farmwald (both named inventors, as well as Rambus founders who own a significant amount of Rambus stock), and the declaration of Mr. Murphy (Rambus's paid expert) for the assertion of "skepticism by many experts in the field." (Rambus's Br. at 19 (citing A2459(¶12) and A2787(¶105).) The Federal Circuit has criticized such non-objective evidence in analogous circumstances. *Phillips v. AWH Corp*., 415 F.3d

[9] To the extent relevant to the analysis of claim 33, all of the other features recited in claims 26 or 29 were known in the prior art as discussed throughout this brief and during the reexamination proceeding.

1303, 1318 (Fed. Cir. 2005); *see also In re Mettke*, 570 F.3d 1356, 1361 (Fed. Cir. 2009); *Finisar Corp. v. DirecTV Group, Inc*., 523 F.3d 1323 (Fed. Cir. 2008).

F. Summary of the Proceeding Prior to this Appeal

During the initial examination, the examiner determined that claims 26, 29 and 33 were patentable over the rejections proposed by Micron. In its appeal to the Board, Micron argued that the examiner erred in withdrawing the rejection of claims 26, 29 and 33 and demonstrated that the prior art rendered obvious the two limitations that Rambus raises before this Court: (1) an operation code including a read instruction and precharge information and (2) a "synchronous dynamic random access memory device." (A2333-50.)

1. Rejections Based on Bennett

With regards to precharge information, Micron has never argued that Bennett directly discloses this limitation but instead that it would have been obvious in light of the combined teachings of Bennett in view of Wicklund, Bowater, or Olson. Importantly, Micron demonstrated that Bennett disclosed a control protocol that uses multiple memory operation codes including basic read operations (A3326; A2285; A1359; A1637-38(95:98-96:42)) and multi-function memory operations, such as a read-modify-write. (A1357.) In addition, Micron demonstrated that the prior art taught that precharge information was well known,

beneficial, and intimately associated with read and write operations. (A1733(2:55-61); A1752(7:54-56; 7:62-65); A1747; A1761; A1764(3:1-13); A1764(3:28-41).)

Thus, for this limitation, the only proposed modification to Bennett is to add an extra field for precharge information into Bennett's existing read operation code. Further, it would have been obvious to include that information in the existing read operation code because precharge information is intimately related to read operations.

Regarding the "synchronous random access memory device" issue, Micron demonstrated that this limitation would have been obvious to one of ordinary skill in the art based on Bennett's clear teachings of synchronous large slow memory compared to synchronous small fast memory. (A1635(92:9-14) and A1733(2:18-23).) The prior art references of record, such as Wicklund and iRAM, plainly show that it was well-known that DRAM was "the most popular form of read/write memory" and that DRAM was known to have larger capacity but slower timing compared to the smaller and quicker SRAM. (A2134 and A1733.)

Thus, for this limitation, the only proposed modification to Bennett is to replace the generic large and slow synchronous memory of Bennett with the most popular form of such memory—DRAM.

2. Rejections Based on iAPX with iRAM

With regards to the precharge information limitation, Micron demonstrated that iAPX, just as Bennett, disclosed sending operation codes using a synchronous protocol. (A2345; A1858; A1983.) Likewise, the prior art teaches the benefit of using precharge information and its relation to read/write operations. (A1761; A1764(3:1-13); A1764(3:28-41).) Thus, for this limitation, the only proposed modification to iAPX is to add an extra field for precharge information into iAPX's existing read operation code. Further, it would have been obvious to include that information is in the existing read operation code because precharge information is intimately related to read operations.

Regarding the "synchronous random access memory device" issue, Micron demonstrated that the combined teachings of iAPX with iRAM render obvious a "synchronous dynamic random access memory device" on a single chip. In particular, iRAM teaches integrating control circuitry onto the same chip as DRAM. (A2343.) Thus, for this limitation the only proposed modification to iAPX is to integrate MCU circuitry onto the same chip as the DRAM.

3. Rejections Based on JEDEC and Park

The '120 Patent purports to claim priority to the parent '898 application, filed April 18, 1990. Despite Micron's showing that claim 33 lacked the required written description (because it did not claim the multiplexed bus interface of the

invention described in the '898 application), the examiner found that the '120 Patent was entitled to the priority date of the '898 application and refused to adopt rejections based on the intervening references, JEDEC and Park. (A1146.)

4. The Board's Decision

In its Decision issued January 19, 2012, the Board affirmed the examiner's decision to adopt the grounds of rejection of claims 1-4, 6, 8-11, 15, 16, 19, and 21-25 and reversed the examiner's decision not to maintain the grounds of rejection for claims 26, 29, and 33. (A69.) The Board made numerous factual findings to support its rejections of claims 1-4, 6, 8-11, 15, 16, 19, 21-26, 29 and 33. Rambus elected not to appeal the Board's factual and legal findings of obviousness on these claims except for claim 33.

With regards to the synchronous DRAM device arguments that Rambus raises with respect to claim 33 in its brief to this Court, the Board held that the examiner erred in not maintaining the obviousness rejection of claims 26 and 29 based on Bennett given that the evidence shows that it would have been obvious to employ well-known DRAM as a substitute for Bennett's large slow memory chip. (A58.) The Board also held that the prior art taught, just as the '120 patent described, that precharging normally occurs at the end of a read or write function, demonstrating the obviousness of banding two related functions into Bennett's

operation code. (A58.) Moreover, the Board found Bennett discloses multiple functions in a single operation code (read-modify-write). (A58.)

Turning to the obviousness of claims 26 and 29 in view of the combined teachings of iAPX and iRAM, the Board also found that iRAM teaches integrating more functions into an integrated memory to relieve a CPU. (A54(¶I1).) The Board further determined that Rambus acknowledged that iRAM "teaches integrating specific functions" and that such functions involve maintaining "a simple DRAM *interface* to relieve the CPU … (I1, I2)." (A60 (citing A2404-2405)(emphasis in original).) In addition, for similar reasons as with the Bennett rejections, the Board concluded that claim 33's limitation of including precharge information in a read operation code was obvious in light of the combined teachings of iAPX with iRAM and Olson. (A62.)

As a secondary basis to support the Board's determination that claim 33 was obvious in light of the prior art of record, the Board construed the language of claim 33 as not providing a new and nonobvious functional relationship between the precharge information and the device recited in claim 26 and 29 in light of the teachings of the prior art. (A59.)

The Board then fully considered the evidence of secondary considerations and concluded that such evidence failed to establish a nexus between the claimed

features associated with claims 26, 29, and 33 and the allegations of success, solving a long felt need, etc. (A63-A65.)

Finally, the Board determined that the '120 patent was entitled to a priority date of April 18, 1990. (A35-39.) The Board refused to review whether JEDEC or Park anticipated claims 26, 29, and 33 of the '120 Patent.

IV. SUMMARY OF THE ARGUMENT

Rambus fails to show that the Board did not rely on substantial evidence when deciding that claim 33 is obvious. The evidence establishes that it was well-known in the art to provide precharge information to a memory device. Moreover, the evidence shows that an obvious way to provide that precharge information to the synchronous memory devices in the Bennett and iAPX systems was to include the precharge information in the operation codes that are already used and disclosed by Bennett and iAPX.

Next, Rambus argues for patentability in light of the recitation of "synchronous dynamic random access memory device" in the preamble of claim 26. Yet, Rambus waived this issue by not appealing the Board's decision that claim 26 is obvious. Even if the issue is not waived, the preamble should not be considered limiting nor would it restrict the claims to a single chip, particular given this Court's prior construction of "synchronous memory device" which is specifically not limited to a single chip. *In re Rambus*, 694 F.3d at 47. Nonetheless,

the evidence in this proceeding demonstrates that single chip synchronous DRAMs were known and certainly would have been obvious in light of the prior art teachings.

However, the Board erred in determining that claim 33 had priority to the April 18, 1990 filing date of the '898 application because the '898 application does not provide written description support for a memory device that does not interface to a multiplexed bus. (A66-68.) The Board therefore erred in not considering JEDEC and Park as anticipating prior art.

V. ARGUMENT

A. Standard of Review

With regards to the adopted rejections, Rambus has the burden to show that the Board committed reversible error. *In re Watts*, 354 F.3d at 1369. This Court reviews the Board's legal conclusion, including obviousness, *de novo* while upholding the Board's underlying findings of fact that are supported by substantial evidence. *In re Gartside*, 203 F.3d 1305, 1316 (Fed. Cir. 2000); *In re NTP, Inc.*, 654 F.3d 1279, 1297 (Fed. Cir. 2011).

In its appeal, Rambus has contested issues directed to what the prior art discloses and the reason to combine references, both of which are a questions of fact that should be reviewed under the substantial evidence standard. *In re Hyatt*, 211 F.3d 1367, 1371 (Fed. Cir. 2000); *Para-Ordnance Mfg. v. SGS Importers Int'l,*

Inc., 73 F.3d 1085, 1088 (Fed. Cir. 1995). "The 'existence of a reason for a person of ordinary skill to combine references' is a question of fact that we review for substantial evidence." *In re Hyon*, 679 F.3d 1363, 1365-66 (Fed. Cir. 2012) (citing *In re Constr. Equip. Co.*, 665 F.3d 1254, 1255 (Fed. Cir. 2011)).

Substantial evidence "is something less than the weight of the evidence but more than a mere scintilla of evidence," *In re Kotzab*, 217 F.3d 1365, 1369 (Fed. Cir. 2000), and "means such relevant evidence as a reasonable mind might accept as adequate to support a conclusion." *Consol. Edison Co. v. NLRB*, 305 U.S. 197, 229 (1938).

B. The Board May Rely On Its Scientific Knowledge In *Inter Partes* Reexamination Proceedings

Throughout its Brief, Rambus argues that the Board improperly substituted its own expertise in determining that claim 33 was rendered obvious by the cited prior art. (Rambus's Br. at 3, 44-45, 47.) Rambus has not provided evidence that the Board substituted its own expertise; Rambus only presumes this because the Board came to a different conclusion than the examiner.

This Court, however, "will not find the Board's decision unsupported by substantial evidence simply because the Board chose one conclusion over another plausible alternative." *In re Jolley*, 308 F.3d at 1320. "[T]he possibility of drawing two inconsistent conclusions from the evidence does not prevent an administrative agency's finding from being supported by substantial evidence." *Consolo v.*

Federal Maritime Comm'n, 383 U.S. 607, 620 (1966). As demonstrated herein, the Board determined that substantial evidence supported a conclusion of obviousness even though the examiner came to a different conclusion.

To the extent the Board did rely on its scientific knowledge, it did so to understand the meaning of prior art as it is required to do by law. *In re Berg*, 320 F.3d at 1315 ("examiners and administrative patent judges on the Board are responsible for making findings, *informed by their scientific knowledge*, as to the meaning of prior art references to persons of ordinary skill in the art and the motivation those references would provide to such persons."). Indeed, "administrative patent judges shall be persons of competent legal knowledge and scientific ability." 35 U.S.C. § 6(a). Moreover, the Board explicitly pointed to undisputed factual findings based on the prior art that support the rationale for obviousness. Accordingly, the Board may – as it has done here – rely on its scientific ability to analyze the meaning of prior art references.

C. The Board Correctly Determined that the Prior Art Rendered Obvious an Operation Code Containing Both a Read Instruction and Precharge Information Based on Substantial Evidence[10]

Rambus argues the Board erred in determining that claim 33 is obvious because the "operation code" limitation must be taught in a *single* reference. (Rambus's Br. at 51-52.) Rambus's standard for determining obviousness is incorrect. Nonobviousness cannot be established by attacking the references individually when the rejection is predicated upon a combination of the teachings of the prior art. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417-18 (2007); *see also In re Merck & Co. Inc*., 800 F.2d 1091, 1097 (Fed. Cir. 1986).

In fact, the reasons to modify or combine the prior art do not have to be expressly disclosed in the prior art at all, let alone in a *single* reference. The Supreme Court in *KSR* stated that "the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR*, 550 U.S. at 418. Thus, the prior art references do not need to

[10] While Rambus's brief first addresses the Board's non-functional descriptive interpretation of "precharge information," that interpretation was raised by the Board as an alternative ground. (A58-59 "[U]nder this *alternative* claim interpretation, claim 33 does not require the memory device of claim 29 to operate any differently" (A59.) Accordingly, Micron will address the argument after it addresses the Board's principal claim construction.

expressly teach an operation code containing both a read instruction and precharge information as urged by Rambus.

Instead, given the prior art before it, the Board need only determine that it would have been obvious to a person having ordinary skill in the art to include a read instruction and precharge information in a single operation code and provide "some articulated reasoning with some rational underpinning" supporting its determination of obviousness. *Id.* (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

Contrary to Rambus's assertions, the Board based its decision on substantial evidence from the record. In particular, the Board relied on at least the following factual findings supported by the prior art:

- "Bennett discloses an operation code…for example, Bennett's read-modify-write operation." (A26.) And that, "Bennett discloses multiple functions in a code (See Bennett Fig. 34 (read-modify-write code signifying multiple functions.))" (A58.)
- "[I]t was known in prior art systems (such as Wicklund's, Bowater's, and Olson's) that 'precharge normally (i.e., when the DRAM is not in page mode) occurs at the end of a read or write function.'" (A26) Further it was an "undisputed finding that a precharge follows a read in the normal non-page mode in prior art systems." (A27.)
- "The two signals [the precharge information and the read/write instruction] were intimately related in the prior art with one normally following the other, thereby rendering the 'banding' of the two in Bennett's operation code obvious, where Bennett bands together other instructions in an operation code such as the 'read-modify-write.'" (A27.)

- "Wicklund shows, in a similar fashion to the '120 patent, that precharge normally (i.e., when the DRAM is not in page mode) occur at the end of a read or write function, showing the obviousness of banding the two related functions into Bennett's write code." (A58.)
- "[S]ending one operation code with information as required to perform certain read operation would have been obvious for the purposes of keeping related read control information together in an existing (or modified) iAPX operation code." (A62-63.)
- "Olson teaches sending precharge information to memory devices" and "the combination of Olson and the iAPX Manual suggests determining 'whether or not to precharge.'" (A62.)

Based on the above substantial evidence, the Board correctly concluded that claim 33 was obvious whereas the examiner did not.

Rambus contends that the Board erred because the declaration of its purported expert, Mr. Murphy, is "unrebutted." (Rambus Br. at 52.) Although Micron did not submit an expert declaration directly in the reexamination,[11] none was required because the teachings in the prior art and other evidence provided any necessary rebuttal. First, the basis for Rambus's reliance on Mr. Murphy is not supported by Mr. Murphy's declaration, namely that "precharge information, if it existed, would have come from within the large memory, while requests to memory…would have been sent across the primary bus from the CPU." (Rambus's Br. at 53 (citing Mr. Murphy at A2480(¶73); A2427-29(¶¶56-59); A2467(¶31); A2470(¶38).)

[11] The record in this proceeding contains numerous expert declarations and testimony from the underlying litigation.

The only paragraph from Mr. Murphy's declarations cited by Rambus that relates to Bennett is ¶73. However, this paragraph is premised on a factually inaccurate theory that the Versatile Bus Interface is on a separate chip than the User memory. (A2480(¶73) (referring to the Versatile Bus Interface as "a separate interface" from the memory module).) That argument was thoroughly addressed in the reexamination proceeding, with the Board finding that Bennett disclosed that the VBI and User memory were on the same chip. (A25 (incorporating by reference '916 Decision at A10009).) Mr. Murphy also asserts that the signals between the Versatile Bus Interface and the User memory would be "asynchronous" (A2480(¶73)), but that is also contradicted by Bennett's express disclosure that the bus between the Versatile Bus interface and the memory is synchronous. (A1640(101:50-54).)

The cited paragraphs of Mr. Murphy's declarations regarding iAPX and iRAM do not even discuss including precharge information in an operation code with a read instruction. (A2427-29(¶¶56-59); A2467(¶31); A2470(¶38).) At most, those statements assert that the operation code in iAPX is received by the MCU rather than directly by the memory and that the MCU would not be integrated with

the memory on a single chip. Thus, these statements only relate to the separate issue of whether iAPX and iRAM teach integrating the MCU and memory.[12]

Furthermore, Mr. Murphy's belief that a prior art CPU would not handle DRAM-specific instructions contradicts the prior art of record, including Bennett, which makes clear that CPUs can and do send DRAM-specific instructions to memory devices. (*See e.g.*, A1734(Bennett at 4:61-62) ("in some computers, [DRAM] refresh is directly controlled by the CPU system."); *see also* A2156 (iRAM discussing CPU control of DRAMs); A1752 (Bowater at 7:62-65 preset time to bring DRAM out of page mode by precharging "is determined under control of the signal inputs *from microprocessor* 110.").)

In addition, Bennett provides an example embodiment of a simple interconnect where the only two devices connected to the Versatile Bus are a processor and a single slave memory device. (A1597(15:42-53) and A1618(57:54-59).) In this simple two-device configuration, the processor must be aware of memory specific attributes, such as page boundaries, since there is no intermediary controller between the processor and the memory device.

[12] As discussed in Sections V.E and V.F below, this Court should not adopt a single chip construction for claim 33 because the "synchronous dynamic random access memory device" term Rambus relies on for this proposition is non-limiting preamble language and, even if it was limiting, it does not require this Court to modify its prior construction of "synchronous memory device" which is not limited to a single chip.

In other words, Rambus has not provided any evidence supporting its conclusory argument that Bennett's processor or iAPX's BIU controller would be unable to provide precharge information to DRAM. Even if Rambus could provide evidence – which it cannot – the Board determined that Bennett's processor and iAPX's controller would not have been required to be aware of all memory attributes, such as page boundaries, to send precharge information after a read in non-page/normal mode. (A27 ("a controller issuing a simple instruction involving a normal read and precharge would not have been required to be aware of page boundaries which might occur in a page mode."); *see also* A29 ("skilled artisans would have recognized that an iAPX modified controller would have had sufficient 'perspective' to send a precharge signal to an integrated DRAM in the same code as the read signal since the precharge signal normally would have followed the controller's read signal in prior art systems…").)

Rambus next argues that "one of ordinary skill in the art looking at Olson, Wicklund, and Bowater would not have tried to combine read and precharge instructions into a single operation code because those references teach away from such a solution." (Rambus's Br. at 53.) However, this Court has held, "[t]he prior art's mere disclosure of more than one alternative does not constitute a teaching away from any of these alternatives because such disclosure does not criticize, discredit, or otherwise discourage the solution claimed." *In re Fulton*, 391 F.3d

1195, 1201 (Fed. Cir. 2004). Rambus cannot point to a single citation from the prior art that teaches away from combining a read instruction and precharge information into a single operation code.

Rather, Micron demonstrated – and the Board found persuasive – the obviousness of combining a read and precharge information. (A58 (citing A2337-40 and A3326-30); A62 (citing A2350).) Micron explained that it would have been obvious to a person of ordinary skill in the art to include precharge information as taught by Wicklund, Bowater, or Olson with a read operation code as taught by Bennett or iAPX. (*See e.g.,* A2287-90.) The basis for these statements is not unsupported attorney argument as Rambus contends, but is expressly provided by the very references relied on for the rejections.

For example, Wicklund's invention used a prediction algorithm directed towards switching between two modes of operation: one that does not automatically precharge and instead leaves data available for a subsequent access (page mode), and one that does automatically precharge and does not leave data available for a subsequent access (normal/non-page mode). (A1733(2:55-61).) With regards to normal/non-page mode, and as acknowledged by the '120 Patent and Rambus's expert, an automatic precharge occurs in normal/non-page mode reads in conventional DRAMs. (A102(10:18-21); A10032; *see also* A10044.)

With regards to page mode, Wicklund discloses that "DRAMs need to be refreshed at regular intervals, so the page mode may need to be interrupted to perform a refresh cycle." (A1733(2:43-45).) To address this issue, Micron argued – and the Board agreed – it would have been obvious to provide an instruction with an operation code to automatically precharge while in page mode to prevent data from being corrupted. (A2287; A58.)

Likewise, Bowater teaches that a row must not be left open too long before it becomes corrupted. (A1752(7:54-8:8.) To prevent corrupted memory, Bowater sets a counter to automatically perform a precharge after a memory access. (A1752 (7:62-65.)) Micron argued that it would have been obvious to include a precharge information as taught by Bowater in an operation code to automatically perform a precharge after a certain length of time in page mode to prevent the memory from becoming corrupted.[13] (A2338; A2289.)

Similarly, Olson describes improving memory operations by instructing the memory whether or not to precharge. Specifically, Olson's memory controller selectively activates control signals MEMPAGE and MEMCYCLE to control precharging of the memory. (A1763(2:40-44); A1764(3:28-30; 3:52-60).) Micron explained – and the Board agreed – that it would have been obvious to send this

[13] Sending a control signal (such as precharge information) with an operation code would not defeat the counter, as Rambus so contends, but rather provides an alternative, obvious solution. The precharge information in Bowater sets a value used by the counter and does not replace the counter. (A1752 (7:62-65).)

beneficial precharge information with the existing operations codes in Bennett or iAPX. (A2339-40; A2350; A58; A62.)

Moreover, sending control information (such as precharge information) using the same operation codes already used in Bennett and iAPX with iRAM would have been one of the "finite number of identified, predictable solutions" for sending such signals, and therefore, would have been obvious to try. *See KSR*, 550 U.S. at 421. In other words, the rejection relies on the existing synchronous communication protocol of Bennett and iAPX and merely modifies that communication to include the beneficial precharge information taught by Wicklund, Bowater, or Olson.

Rather than address this rejection, Rambus improperly argues that asynchronous protocol used by Wicklund, Bowater, or Olson to transmit precharge information could not work as required by the claim. Rambus, however, has not provided any evidence that it would have been impossible or even difficult to implement known memory controls in asynchronous systems into a synchronous system. Nor has Rambus provided any evidence that precharge information was only useful for asynchronous memories. Instead, the evidence discloses that synchronous memories (e.g., Bennett or iAPX) use read operations just as asynchronous memories and that synchronous memory would benefit from using precharge information in the same way as asynchronous memory benefitted.

Lastly, Rambus argues that Bennett's read-modify-write operation does not actually contain "two independent and distinctly identifiable instructions." (Rambus's Br. at 57.) In sum, Rambus argues that Bennett's read-modify-write instruction does not provide a "bundled" operation code, but rather "reads the data in that memory address and writes a new value to that same address." (Rambus's Br. at 57.) Yet, Rambus appears to concede that two operations are occurring: a read and a write. Nothing in the claim requires the operation code to have "independent and distinctly identifiable instructions," and Rambus does not explain what that new limitation would mean in light of the specification. Rambus may not properly insert "independent and distinctly identifiable instructions" into the claim. *See Superglide Corp. v. DirecTV Enterprises, Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004).

Even if Rambus were correct that Bennett did not disclose any operation codes with multiple functions, the findings of the Board and teachings of the prior art amply support that modifying Bennett's operation code to include precharge information would have been a predictable task to one of ordinary skill in the art that would have resulted in providing the well-known benefits of precharge to Bennett's read operation codes.

Undeniably, the prior art disclosures and other evidence constitute "substantial evidence," or "relevant evidence as a reasonable mind might accept as

adequate to support a conclusion." *Consol. Edison Co.*, 305 U.S. at 229. The fact that the examiner came to a different conclusion than the Board on the same evidence is not legally relevant. *In re Jolley*, 308 F.3d at 1320. Thus, Rambus's argument that the Board did not base its decision on substantial evidence is incorrect in light of the very specific factual findings the Board relied on to support its Decision.

D. The Board Did Not Err in Construing "Precharge Information" Recited in Claim 33 as Obvious "Nonfunctional Descriptive Material"

If the Court reaches this issue, it is important to note that Rambus appears to misconstrue the Board's position. The Board did not conclude that the "precharge information" limitation "need not be present in the prior art" as Rambus suggest (Rambus Br. at 48), but rather that the broad nonfunctional descriptive nature of the limitation makes the claim limitations even more obvious in light of the prior art than if the claim were construed more narrowly. (A59; A62 ("Such nonfunctional descriptive material…fails to render claim 33 patentably distinct over iAPX and iRAM (i.e., with or without the added teachings of Olson)").) Thus, Rambus's reliance on cases that all elements of a claim have meaning is off point because the Board never concluded otherwise.

The Board's broad alternative construction is based on the fact that the "precharge information" recited in claim 33 has no functional relationship to the

claimed apparatus because the memory device takes no action based on the "precharge information." This is similar to this Court's decision in *In re Ngai* finding no patentability when "the printed matter [a set of instructions] in no way depends on the [claimed] kit, and the kit does not depend on the printed matter." *In re Ngai,* 367 F.3D 1336, 1339 (Fed. Circ. 2004). Here, the "precharge information" does not depend on the memory device and the memory device does not depend on the "precharge information."

Rambus acknowledges that claim 33 does not "recite the act of precharging the sense amplifiers" but contends that receiving precharge information in the same operation code as a read instruction "changes the timing of bus access compared to the prior art and significantly improves the efficiency of the system." (Rambus Br. 49).[14] However, claim 33 is an apparatus claim directed to a memory device interface rather than a claim directed to a system or method of using the memory device interface. Thus any improvement to the "system" by using an operation code that included precharge information and a read instruction is not attributable to the claimed memory device. This is particularly evident in that the operation of the claimed memory device does not change whether or not it receives any precharge information.

[14] Not surprisingly, Rambus takes the exact opposite view with respect to the prior art in arguing that no one of ordinary skill in the art would be motivated to improve prior art synchronous memories by using existing operation codes to transmit well-known precharge information.

E. Rambus Waived Its Right to Contest the Board's Factual and Legal Findings that the Limitations Recited in Claims 26 and 29 Are Rendered Obvious

Rambus has only appealed the Board's finding of obviousness of claim. By doing so, Rambus has waived its right to ask this Court to review the Board's findings relative to claims 26 and 29. Since the only occurrences of the term "synchronous dynamic random access memory" or "synchronously" are by virtue of claims 26 and 29, Rambus has waived its right to contest the Board's findings that the prior art renders the limitations of claims 26 and 29 obvious.

Because Rambus has not appealed them, the Board's factual findings and legal analysis as to why claims 26 and 29 are obvious are now final. As Rambus had a full and fair opportunity to present its case on the issues related to these claims, but chose not to, it cannot contest the Board's findings on identical issues in a later proceeding. *Compare Jet, Inc. v. Sewage Aeration Sys*., 223 F.3d 1360, 1366 (Fed. Cir. 2000). If this Court were to now address the issues for claim 33 that are now final for claims 26 and 29 and reach a different obviousness conclusion than the Board, then the result would be a final decision that the *exact* same limitations are both obvious and non-obvious over the *exact* same prior art rejections. Such a contradictory outcome would only cause additional confusion and litigation and is exactly why this Court should decline to review these now final issues.

The only limitation added in claim 33 is the inclusion of "precharge information" in the operation code, and this Court should not entertain Rambus's arguments unrelated to that limitation.

F. The Board Correctly Determined that the Prior Art Rendered Obvious a Synchronous Dynamic Random Access Memory Device Based on Substantial Evidence

If the Court reaches this issue, it should find the term "synchronous dynamic random access memory device" is not limiting because it is only recited in the preamble and is not "essential" to the body of the claim. *American Medical Systems, Inc., v. Biolitec, Inc*., 618 F.3d 1354, 1358 (Fed. Cir. 2010). The body of the claim is directed to an interface for a memory device and the type of memory used (e.g., dynamic random access) is not necessary to define the claimed memory device interface.

If the Court finds the preamble limiting, Rambus's argument that claim 33 requires a DRAM chip is inconsistent with the claim language and this Court's prior decisions. The terms "synchronous," "dynamic," "random," and "access" alone or in combination, simply modify the term "memory device." This Court already has held that "memory device" is not limited to a single chip. *In re Rambus*, 694 F.3d at 47 ("we construe a 'memory device' as a component of a memory subsystem, not limited to a single chip, where the device may have a controller that, at least, provides the logic necessary to receive and output specific

data, but does not perform the control function of a CPU or bus controller").[15] The District Court also viewed these terms as merely "modify[ing] the phrase 'memory device.'" (A3152-53.)

Rambus argues that the Board's determination that synchronous DRAMs would have been obvious is unsupported by substantial evidence because none of the prior art references discloses synchronous DRAMs. (Rambus's Br. at 60.) Again, Rambus is merely attempting to attack the references individually, rather than addressing what the combination of the references as a whole would have taught one of ordinary skill in the art. *In re Merck*, 800 F.2d at 1097.

The Board based its determination on the undisputed disclosures of the prior art of record, including:

- "DRAMs were a well-known, if not dominant, form of a memory chip device at the time of the invention." (A56.)
- "[T]he various discussion of memory chips as preferred over cards in Bennett and other related teachings relied upon in Micron's Briefs would have rendered obvious employing such a ubiquitous device as a DRAM." (A57.)
- "These speed and power features of chips…also evidence an 'implicit motivation' for obviousness of using a chip…such as a known DRAM chip." (A57.)
- "Bennett's generic synchronous single-chip memory disclosure and Rambus's concession that DRAMs were a well-known, if not

[15] In a related appeal Rambus has argued that this is a new construction not argued before by Micron. Yet, Micron argued in its appeal to the Board that "none of the words 'synchronous,' 'dynamic,' 'random,' [and] 'access'…alone or in combination limit claim [26] to a single chip." (A3319.)

dominant, type of memory chip…render obvious the combination" (A21.)

- "Bennett is not only forward looking and contemplates large address space in future memory chips, but Bennett also specifically contemplates less address space in chips having a small number of pins." (A21-22.)

- "The iRAM Manual teaches shifting some of the CPU tasks to…an integrated RAM, relieving the CPU of hardware functions….In other words, the iRAM Manual teaches integrating more functions into a single device, an integrated memory, to relieve the CPU." (A54 (citing A2134 and A2155-57).)

- "[T]he iRAM reference shows that prior to the claimed invention, chip designers were integrating typical control functions into DRAM memories to free controllers (*e.g.,* a CPU), of those memory control tasks, thereby minimizing cost, optimizing timing, and simplifying memory systems by eliminating such CPU tasks" (A59-60 (citing A2346, A2134, and A2155).)

- "[I]t would have been obvious based on iRAM to integrate known functions of the iAPX memory module into a single DRAM chip." (A59 citing A2343-45).)

- "[T]he iRAM solution suggests a system of iRAMs and a processor, thereby indicating some processor control…and suggesting a simple 'integrated solution' involving an 'MCU interface.'" (A60.)

- "In sum, this record show little, if any, dispute over the fact that the iRAM Manual suggests integrating some control functions onto a DRAM chip to create an integrated synchronous memory chip having advantageous memory control and CPU interface features." (A61.)

Other evidence in the record also supported the Board's determination that synchronous DRAMs were known and would have been obvious. (A2134; 2139; *see* A10047; A10252 at ¶22.) Accordingly, the Board correctly determined that a synchronous DRAM would have been obvious in light of the prior art disclosures.

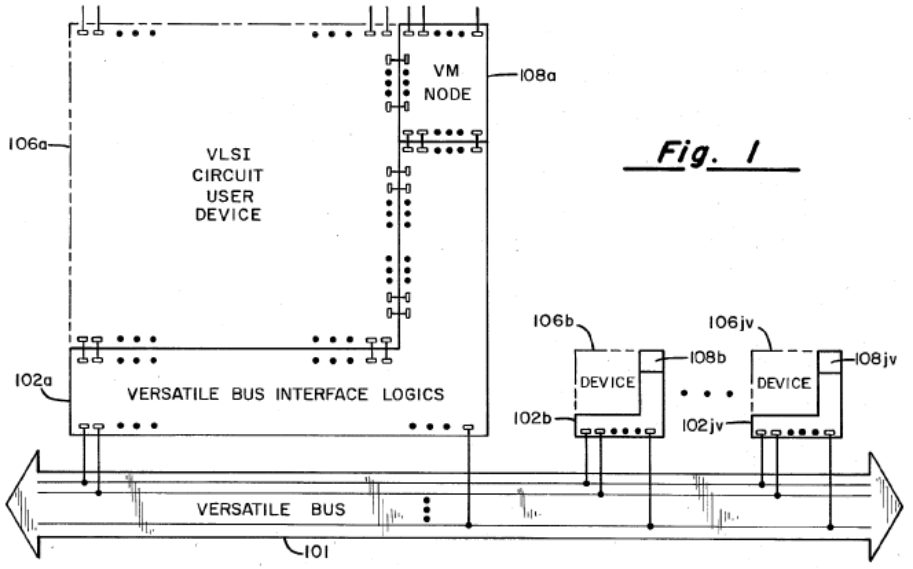
Rambus cannot provide any evidence that the Board erred in this determination of obviousness or point to any evidence that would reasonably lead this Court to a different conclusion.

Notwithstanding the overwhelming evidence of record that a synchronous DRAM would have been obvious, Rambus continues to argue the merits of this determination to this Court. Specifically, Rambus argues that "Bennett did not envision attaching a single DRAM chip directly to the primary bus…." (Rambus's Br. at 61.) In making this argument, Rambus ignores the claim language and the substantial evidence to the contrary.

Bennett's Versatile Bus is purposefully designed to be a flexible standard interface that provides interconnection to a myriad of devices. (A1595(12:14-25).) In fact, the system of Bennett is fully aware that certain User devices like memory will be "crude[]," while other User devices like CPUs will be "sophisticated," but that both are designed to connect to the same Versatile Bus. (A1609(40:55-59).) Thus, the Versatile Bus in Bennett is designed to be connected to User memory. In fact Bennett even provides an example where the only two devices connected to the Versatile Bus are a processor and a single User memory chip. (A1597(15:42-53); A1618(57:54-59).) Thus, Rambus's "single DRAM chip" argument contradicts Bennett's disclosure.

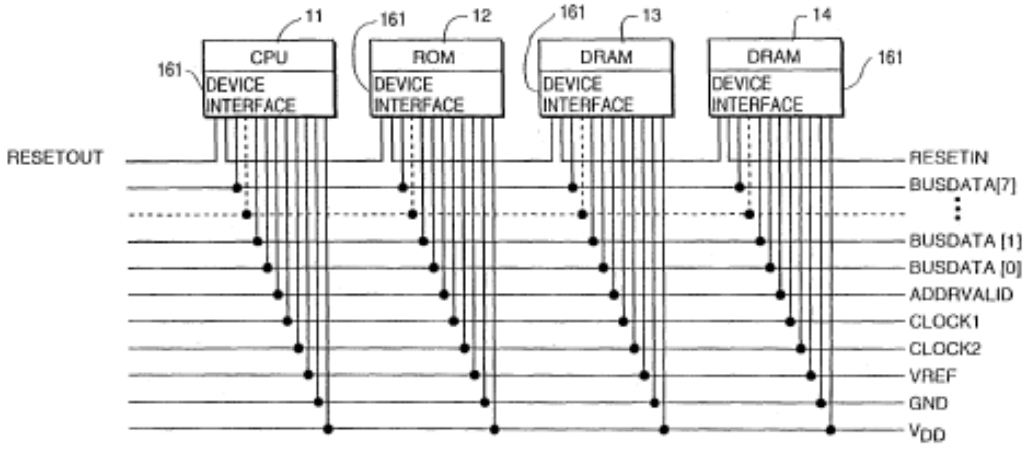
Rambus further relies on Bennett's disclosure of "a large memory *up to* 2^{32} addresses of 32 bit words" despite the fact that "up to" means the large memory could have a much smaller address space. (Rambus Br. at 61.) Further, Rambus's argument is based on a theory that Bennett uses memory cards to hold an address space of that size instead of memory chips, even though Bennett disparages memory cards. (A1594[9:36-50].)

In addition, the Board based its determination on the finding that Bennett discloses *a user device* that is connected to Bennett's Versatile Bus: "the Versatile Bus Interface Logics should offer ... [an] interface to the user devices (usually upon the same chip substrate." (A1596(14:21-24); A57 (citing A2333-37).) In other words, both a Versatile Bus Interface and memory (for example, DRAM) are included on the same single chip that is connected to Bennett's Versatile Bus as illustrated in Figure 1:



(A1046)

In fact, Bennett's Figure 1 is nearly identical to Figure 2 from the '120 Patent where Bennett's User device corresponds to the '120 Patent's CPU, ROM, and DRAM and the Versatile Bus Interface corresponds to the '120 Patent's Device Interface.



'120 Patent Figure 2 (A84)

Next, Rambus argues that the only memory disclosed in Bennett is "large memory" which "would have contained *many* DRAM chips connected to a controller on a separate, secondary bus and operated asynchronously." (Rambus's Br. at 60-61.) Relatedly, Rambus argues that a clock would not have been provided to a DRAM. (Rambus's Br. at 65.) These arguments are meritless for at least two reasons.

First, Rambus's argument relies on a new claim construction of "synchronous dynamic random access memory device" that limits the term to just the memory itself. However, the term is not a memory but a "memory device"

which would include at least the other elements on the same chip as the memory, such as Bennett's Versatile Bus Interface Logics. Rambus has identified nothing in the '120 Patent that would require the memory itself to receive a synchronous signal so long as the chip's external interface containing the memory device receives a synchronous signal. (*See* A82 (Figure 2 of the '120 patent only depicts a clock going to the device interface and not the DRAM).) Furthermore, expert declarations support that the term "synchronous DRAM" describes "a synchronous interface to an asynchronous DRAM core." (A10253-54 at ¶26.)

Rambus's argument to exclude the Versatile Bus Interface Logics is inconsistent with the Court's construction that a memory device may contain some control and interface circuitry. *In re Rambus*, 694 F.3d at 47. Therefore, Bennett teaches this limitation since it is undisputed that the single chip containing the Versatile Bus Interface and the memory in Bennett receives a synchronous signal. (Rambus's Br. at 32 (Bennett "discloses many possible 'Users' that can be connected to the synchronous Versatile Bus …").)

Second, even assuming Rambus's new claim construction was correct, Bennett would still teach the limitation because Bennett explicitly discloses that the communication between the Versatile Bus Interface Logics and the User memory is synchronous. (A1640(101:50-54)("The timing diagram of Fig. 52a firstly shows as reference the signals (H) ϕ1 and (H) ϕ2 to which all

communication between the Versatile Bus Interface Logics and the User, and upon the Versatile Bus, is synchronously referenced.").) Thus, the User memory itself receives synchronous signals.

Therefore, Bennett teaches a "synchronous dynamic random access memory device," regardless of whether the claim requires the single chip containing the DRAM and Versatile Bus Interface to receive synchronous signals or whether the claim requires the User memory itself to receive synchronous signals.

Lastly, Rambus's contention that combination of iAPX with iRAM does not render obvious a synchronous random access memory device is based on its argument that neither iAPX nor iRAM discloses synchronous chips. Again however, this assertion is based on Rambus's flawed premise that the memory array must be synchronous rather than the memory device (which encompasses both the MCU and the memory array). This court has already determined that the MCU and memory array are a "synchronous memory device" and there is no dispute that iAPX discloses using DRAM. *In re Rambus*, 694 F.3d at 50-51. Thus, this court should also find that the MCU and the memory array constitute a "synchronous dynamic random access memory device." Further, to the extent necessary, iRAM also teaches a memory that "provid[es] data" synchronously with an external clock. (A2139 and A28.)

Finally, Rambus's argues that the proposed integration would render iAPX "inoperable" due to changes in fault tolerance features such as error checking and correction (ECC) and redundant DRAMs. (Rambus Br. 67.) However, iAPX never describes fault tolerance features as necessary and ECC can be disabled. (A1786; A1800; A1987.)

Though the Board came to a different conclusion than the examiner, this is irrelevant as long as there is substantial evidence supporting the Board's determination. *See In re Jolley*, 308 F.3d at 1320. Rambus's argument that the Board did not base its Decision on substantial evidence is incorrect in light of the very specific factual findings the Board relied on to support its Decision.

G. Alternatively, the Board Erred in Not Adopting the Anticipation Rejections Based on JEDEC and Park

Alternatively, in addition to the rejections discussed above, JEDEC and Park anticipate claim 33 of the '120 Patent.[16] The Board and the examiner erred in determining that claim 33 is entitled to the earlier filing date of the '898 application, which was the only basis for not adopting Micron's proposed rejections based on JEDEC and Park. As Micron argued on appeal to the Board, claim 33 is not entitled to an earlier filing date because claim 33 is so different

[16] These same alternative grounds for affirmance apply as well to claims 26 and 29; however, Rambus has not appealed the PTO's rejection of those claims.

from the "invention" described in the specification of the original '898 application that the right of priority to those earlier applications was lost. (A2486-2624.)

Claim 33 is not expressly limited to the type of "bus" over which the memory device communicates with the rest of the system. The '898 parent application, to which the '120 Patent purports to claim priority, is explicit that the bus must be a "multiplexed" bus, where the various address, data, and control information is carried over the same plurality of bus lines, and is "multiplexed" so that the different information is carried at different times. Accordingly, Micron showed that because claim 33 broadly encompasses any "bus" that would connect the memory to the rest of the system, those claims have no written description support in—and no priority to—the '898 parent application, which describes only a "multiplexed" bus for reading or writing data.

In rejecting Micron's arguments, the Board based its decision on its belief that the priority determination was controlled by the claim construction adopted by this Court in *Infineon*, 318 F.3d at 1094-95. (A66.) That belief is incorrect. In a post-*Infineon* case involving priority issues as raised in this appeal, this Court stated: "*Though it would certainly be reasonable to conclude that Rambus's claims do not meet the written description requirement on the basis of ICU Med*., that argument was presented to the jury and rejected by it." *Hynix Semiconductor Inc. v. Rambus Inc.,* 645 F.3d 1336, 1352-1353 (Fed. Cir. 2011) (referring to *ICU*

Medical, Inc. v. Alaris Medical Systems, Inc., 558 F.3d 1368 (Fed. Cir. 2009) (emphasis added)).

The Court's statements in *Hynix* show that the *Infineon* claim construction ruling is not dispositive of the written description priority issue. As in *Hynix*, and as further detailed below, "it would certainly be reasonable to conclude that Rambus's claims do not meet the written description requirement on the basis of *ICU Med*." *Hynix,* 645 F.3d at 1352-53. Moreover, unlike in *Hynix*, there is no jury verdict that constrains this Court's determination of the priority issue.

As shown below, the evidence demonstrates that claim 33 of the '120 Patent is not entitled to the filing date of the '898 application. Thus, JEDEC and Park are prior art and should have been applied by the Board to reject claim 33.

1. The Board Relies on an Improper Legal Standard for Priority Written Description

The Board upheld the examiner's determination of priority based on this Court's decision in *Infineon* that the claim construction of "bus" was not limited to a multiplexed bus. (A66-68.) Although Micron argued that *Infineon* did not apply to the section 112/120 issue in this proceeding, the Board improperly concluded:

> Micron's contentions are unconvincing to show that *Infineon* was wrongly decided or would somehow require reaching a different result based on a written description priority analysis as opposed to its claim construction analysis. (A66.)

Nevertheless, the Board is incorrect that an analysis of written description priority would have the same result as this Court's claim construction analysis in *Infineon*. This Court recognizes that a patentee may prevail on a broad claim construction, only to have the patent later declared invalid for failure to include a written description of sufficient breadth. *See, e.g., Ariad Pharms., Inc. v. Eli Lilly & Co.*, 560 F.3d 1366, 1377 (Fed. Cir. 2009). Notably, in deciding *Hynix* this Court cited *Infineon* only with respect to claim construction and not regarding written description. *Hynix,* 645 F.3d at 1349-53. Thus, even if *Infineon's* claim construction is correct that "bus" is not limited to a "multiplexed bus," that fact alone does not mean the specification of the '898 application provides written description support for a non-multiplexed bus as determined by the Board.

2. Proper Legal Standard for Determining Priority Written Description

In order for a patent claim to receive the benefit of an earlier filing date under 35 U.S.C. § 120, the invention as claimed must have been "disclosed in the manner provided by the first paragraph of section 112 of this title [in the earlier application]." 35 U.S.C. § 120; *see also Tronzo v. Biomet, Inc.,* 156 F.3d 1154, 1158 (Fed. Cir. 1998). Courts have found three requirements encompassed by the language of 35 U.S.C. § 112, ¶ 1: "[1] describe, [2] enable, and [3] set forth the best mode." *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co*., 535 U.S. 722, 736 (2002); *Ariad*, 598 F.3d 1336, 1344-1345 (Fed. Cir. 2010) (*en banc*).

The issue here is whether the "invention" recited in claim 33 was described in the manner required by § 112 in the original '898 application in order to establish priority under § 120.

In *ICU Medical*, the Federal Circuit addressed a claim that failed to recite an element of the invention described in the specification. The patent at issue in *ICU Medical* was directed to a medical valve. *ICU Med.*, 558 F.3d at 1377. All of the valves described in the patent specification included a "spike"; however, the relevant claims did not require a spike. *Id.* The Court referred to the "claims as spikeless not because they exclude the preferred embodiment of a valve with a spike but rather because these claims *do not include a spike limitation*." *Id.* The patentee argued that claims were "neutral regarding whether the valve must include a spike," and therefore, covered either the presence or absence of a spike. *Id.* The Court found that the patentee violated the written description requirement by attempting to broaden the claims to exclude an element of the disclosed invention:

> *[The] asserted spikeless claims are broader than its asserted spike claims because they do not include a spike limitation*; these spikeless claims thus refer to medical valves generically—covering those valves that operate with a spike and those that operate without a spike. *But the specification describes only medical valves with spikes*. *Id*. at 1378.

Similarly, in *LizardTech, Inc. v. Earth Resource Mapping, Inc.*, 424 F.3d 1336 (Fed. Cir. 2005), the Court was faced with two similar independent claims (claims 1 and 21). *Id.* Claims 1 and 21 were both directed to image processing on a

computer using a discrete wavelet transformation (DWT) based compression process. *Id.* at 1340. Nevertheless, while claim 1 recited the specific way to calculate the DWT that was described in the specification, claim 21 recited the process generically. The Court affirmed the invalidity of claim 21 based on a violation of the written description requirement because claim 21 as drafted was broader than the specification could support. *Id.*

A key factor discussed by the Court in holding claim 21 invalid was that the broad generic claim 21 covered "prior art that suffers from precisely the same problems that the specification focuses on solving." *Id.* at 1343-44. In other words, by describing how the disclosed invention differs from the prior art, a specification defines both what the disclosed invention is, and importantly, what it is not.

3. The Memory Device "Invention" Disclosed in the '120 Patent Requires an Interface to a Narrow Multiplexed Bus

In resolving the issue of whether claim 33 of the '120 Patent is entitled to claim priority to the '898 application, the first step is to determine what memory device "invention" is described in the '898 application. *Tronzo*, 156 F.3d at 1159.

As the following analysis shows, the "invention" of the '898 application required a bus interface that includes signal lines over which substantially all address, data, and control information is carried. Because the address, data, and control information is carried over the same lines, the information must be "multiplexed," or "time shared," in that each of the different types of information

(address/data/control) is sent over the common set of bus lines at different times. (*See* A2530; *see also* A2617(Fig.6).) The '898 application describes in detail this "multiplexed bus" invention.

First, the "Summary of the Invention" explains that the "present invention" requires the disclosed narrow multiplexed bus:

> The *present invention* includes a memory subsystem comprising at least two semiconductor devices, including at least one memory device, *connected in parallel to a bus, where the bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by said memory devices*, where the control information includes device-select information and *the bus has substantially fewer bus lines than the number of bits in a single address, and the bus carries device-select information without the need for separate device select lines connected directly to individual devices*.

(A2495). Indeed, the very next paragraph describes how the prior art must be "modified" in accordance with the invention to include an interface to the "new bus" (A2495-96); (A2496-97 ("New bus interface circuits *must be added* and the internals of prior art DRAM devices *need to be modified* so they can provide and accept data to and from the bus at the peak data rate of the bus.").) The '898 application also explains how the multiplexed bus interface is required for DRAM and other devices in "the system of this invention." (A2496.)

Thus, the new bus interface uses the same bus lines to carry address, control, *and* data information. Moreover, the patent excludes the possibility of signal pins

(connections to signal lines) other than to the address/control/data bus lines. The Detailed Description also consistently describes the "present invention" as requiring devices adapted to interface to this narrow multiplexed bus. (A2499.)

Although the '898 application describes certain embodiments of the multiplexed bus interface as "preferred" or "examples" (*see*, *e.g.*, A2497 (providing specific stub capacitances and inductances); A2496 (using 40 bit addresses)), the '898 application *never* describes the narrow multiplexed bus interface itself as merely preferred or exemplary. Nor does the '898 application describe any alternative bus interface structure.

All the original claims of the '898 application that are directed to sending or receiving data are limited to devices adapted to interface to the narrow multiplexed bus by reciting a "bus including a plurality of bus lines for carrying substantially all address, data and control information needed by said memory device." (*See*, *e.g.*, A2551 (claim 1); *see also* A2553-2606 (claims 13, 25, 46, 56, 68, 82, 95, 97, 103, 106, 108, 111, 114, 116, 118, 121, 124, and 135).)

Indeed, only two original independent claims did not expressly describe interfacing to the multiplexed bus: claim 73, which is directed to the specific early/late clocking scheme disclosed in the '898 application, and claim 91, which is directed to the specific packaging scheme disclosed in the '898 application. That these claims do not recite the multiplexed bus is irrelevant, however, because

neither claim is directed to sending or receiving data to or from a memory device. The '898 application described the specific early/late clock and specific packaging scheme described in the specification as separate inventions. (*See* A2493 ("The clocking scheme used in this invention has not been used before"); A2494 ("Another object of this invention is to provide a clocking scheme to permit high speed clock signals to be sent along the bus with minimal clock skew between devices."); A2530 ("Low Power 3-D Packaging" and "an innovative 3-D packaging technology").)

4. The Prior Art to the '898 Application Was Distinguished Based on the Bus and Interface Structure

In addition to the above passages describing the "invention" disclosed in the '898 application, a second important source of information comprises the '898 application's description of what the disclosed invention *is not*. *LizardTech*, 424 F.3d at 1343-44. In the Background of the Invention, the applicants distinguished the disclosed bus from the prior art by asserting that the new bus can transmit all address, data, and control information over the same bus lines whereas the prior art relied on separate bus lines. (A2491).

The '898 application also includes a "Comparison With Prior Art" section, in which purported differences between the disclosed invention and various prior art references are discussed. All but one reference is distinguished on the basis that they do not disclose a bus that handles all the signals, i.e., a multiplexed bus.

(A2491-94; (*e.g.*, in distinguishing U.S. Patent No. 3,821,715 to Hoff *et al.*, the application states, "*most important, not all of the interface signals between the devices are bused* (the ROM and RAM control lines and the RAM select lines are point-to-point)").)

The only prior art reference for which a bus structure was not discussed is U.S. Patent No. 4,247,817 to Heller, which related to the clocking scheme of the '898 application, rather than the transfer of address/data/control information. (A2493.) As discussed above, the clocking scheme was described as a separate inventive concept from the interface to the new multiplexed address/data/control bus. (*See* A2493-94.)

In fact the applicants conceded that disclosed features of the '898 application had been used in the prior art, "but never in conjunction with *the bus architecture of this invention*." (2547.) These consistent descriptions of the prior art and how the "invention" differed from the prior art demonstrate that the invention described in the '898 application for reading and writing data required an interface to a narrow multiplexed bus.

Because claim 33 does not limit the way in which the recited memory device communicates with the rest of the system and is not limited to the "multiplexed bus" as described in the '898 patent, claim 33 does not have written description support in the '898 application. As a result, Rambus cannot claim priority to the '898 application, JEDEC and Park are prior art, and the Board erred in not applying those references against claim 33.

VI. CONCLUSION

The Board's decision that claim 33 of the '120 Patent is rendered obvious by Bennett in view of Wicklund, Bowater, or Olson or iAPX with iRAM in view of Olson should be affirmed. As demonstrated above, substantial evidence supports the Board's factual findings, and the Board's obviousness conclusions are correct as a matter of law.

Alternatively, Micron respectfully requests that this Court reverse the Board's determination that claim 33 of the '120 Patent is entitled to the benefit of the earlier filing date and remand to the Board for consideration of JEDEC and Park as prior art.

Dated: August 28, 2013

Respectfully submitted;

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RAMBUS, INC. v MICRON TECHNOLOGY, INC., 2013-1339

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August 28, 2013

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